What is claimed is:

Sub A5

1. A method for forming bonding pads of a semiconductor substrate comprising the steps of:

Providing top layer metal for interconnecting lines and top level metal for bond pads said top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the top level metal being separated by intra-layer dielectric;

Depositing a passivation layer over said top-level metal and over the exposed surface of said intra-level dielectric;

Depositing a layer of photosensitive polyimide over said passivation layer;

Patterning and etching said layer of photosensitive polyimide thereby forming a pattern for said bonding pads;

Patterning and etching said passivation layer thereby exposing said bond pad;

Curing and cross-linking said photosensitive polyimide.

2. The method of claim 1 wherein said top level metal contains Aluminum.

3. The method of claim 1 wherein said top level metal contains aluminum/copper (Al/Cu) alloy.

4. The method of claim 1 wherein the thickness of said bond pad is the thickness of said top level metal said thickness being within the range of between 4000 and 8000 Angstroms.

Sub A6

5. The method of claim 1 wherein said passivation layer is a first passivation layer of Plasma Enhanced oxide deposited to a thickness of about 2000 Angstrom over which a second passivation layer of Plasma Enhanced Si_3N_4 is deposited to a thickness of about 7000 Angstrom.

6. The method of claim 5 wherein said first passivation layer is deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 2.0 and 2.8 Torr for the duration between about 8 and 12 seconds.

7. The method of claim 5 wherein said second passivation layer is deposited using PECVD technology at a temperature between about 350 and 450 degrees C. with a pressure of between about 4.0 and 5.0 Torr for the duration between about 50 and 60 seconds.

Sub A7

8. The method of claim 1 wherein the thickness of said photosensitive polyimide is within the range of between 5.0 and 9.5 um Angstrom after deposition of said photosensitive

polyimide whereby shrinkage of up to 40% of said thickness could occur after curing of said layer of photosensitive polyimide.

9. The method of claim 1 wherein said patterning said layer of photosensitive polyimide is creating a pattern that is above and mates with said plurality of bond pads.

10. The method of claim 1 wherein said etching said layer of photosensitive polyimide is etching through said photosensitive polyimide down to the surface of said passivation layer thereby removing said photosensitive polyimide above said bond pads.

11. The method of claim 1 wherein said patterning and etching of said photosensitive polyimide is achieved cross-linking with ultra-violet radiation through a mask while masking from UV exposure polyimide regions that are above and mate with said bond pads and further dissolving away in a solvent the non-cross-linked polyimide over the bond pads.

12. The method of claim 1 wherein that portion of said photosensitive polyimide that remains after completion of said patterning and etching said photosensitive polyimide is not removed but is left in place to serve as a stress buffer and to

thereby provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching.

13. The method of claim 1 wherein said patterning and etching said passivation layer is removing said first and said second passivation layer above and to the top metal of said bond pads.

14. The method of claim 13 wherein said etching said first passivation layer uses Ar/CF_4 as an etchant at a temperature of between about 120 and 160 degrees C. and a pressure of between about 0.30 and 0.40 Torr for a time of between about 33 and 39 seconds using a dry etch process.

15. The method of claim 13 wherein said etching said second passivation layer uses He/NF_3 as an etchant at a temperature of between about 80 and 100 degrees C. and a pressure of between about 1.20 and 1.30 Torr for a time of between about 20 and 30 seconds using a dry etch process.

16. The method of claim 1 wherein a base layer of SiO_2 is created on the top surface of said substrate said base layer to be created prior to the creation of said top level metal layers

thereby cushioning the transition of stress between the silicon substrate and said top level metal layers.

17. The method of claim 1 wherein said top level interconnecting metal and top-level bond pad metal are formed within or on top of any layer of a semiconductor device other than or in addition to said semiconductor substrate.

18. The method of claim 1 wherein said top level interconnecting metal and top-level bond metal are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed.

19. The method of claim 1 wherein said curing and cross-linking said photosensitive polyimide is in a N_2 gas ambient at a temperature of between about 300 and 400 degrees C. for a time period between about 1.5 and 2.5 hours.

20. A method of forming planarized bonding pads within the structure of a semiconductor device comprising the steps of: providing a semiconductor substrate said semiconductor substrate to contain electrical circuits or other electrical functional components;

providing a wiring layer having wiring and having a plurality of bond pads, the wiring of said wiring layer being directly connected to said bond pads in addition to being connected to said electrical circuits or other electrical functional components within said semiconductor substrate, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, said wiring and said bond pads being separated by intra-layer dielectric;

depositing a layer of top metal over said bonding pads thereby depositing the bonding pad metal;

depositing a passivation layer over said top level metal interconnecting lines and over said top level metal bond pads and over the exposed surface of the intra-level dielectric thereby shielding said bonding pads from damage during subsequent packaging operations;

depositing a layer of photosensitive polyimide over said passivation to a thickness within the range of between 5.0 and 9.5 um Angstrom;

patterning and etching said layer of photosensitive polyimide thereby forming a pattern of photosensitive polyimide said pattern being identical to the pattern of said bond pads;

etching said layer of photosensitive polyimide thereby removing said photosensitive polyimide above said planarized bond pads; and

curing and cross-linking said photosensitive polyimide thereby protecting the underlying circuitry.

21. The method of claim 20 wherein said top level metal contains aluminum.

22. The method of claim 20 wherein said top level metal contains aluminum/copper (Al/Cu) alloy.

23. The method of claim 20 wherein the thickness of said bonding pad is the thickness of said top level metal said thickness being within the range of between 4000 and 8000 Angstroms.

24. The method of claim 20 wherein said passivation layer is a first passivation layer of Plasma Enhanced oxide deposited to a thickness of about 2000 Angstrom over which a second passivation layer of Plasma Enhanced Si_3N_4 is deposited to a thickness of about 7000 Angstrom.

Sub A16

25. The method of claim 20 wherein said patterning said layer of photosensitive polyimide is creating a pattern that is above and mates with said plurality of bond pads.

26. The method of claim 20 wherein said etching said layer of photosensitive polyimide is etching through said photosensitive polyimide down to the surface of said bond pads.

Sub A17

27. The method of claim 20 wherein that portion of said photosensitive polyimide that remains after completion of said patterning and etching said photosensitive polyimide is not removed but is left in place to serve as a stress buffer and to thereby provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching.

28. The method of claim 20 wherein said patterning and etching said passivation layer is removing said passivation layer above and to the top metal of said bond pads.

29. The method of claim 20 wherein a base layer of SiO_2 is created on the top surface of said substrate said base layer to be created prior to the creation of said top level metal thereby

cushioning the transition of stress between the silicon substrate and said wiring layer.

30. The method of claim 20 wherein said curing and cross-linking said photosensitive polyimide is in a N_2 gas ambient at a temperature of between about 300 and 400 degrees C. for a time period between about 1.5 and 2.5 hours.